**DEREE COLLEGE SYLLABUS FOR:**

**ITC 2186 COMPUTER SYSTEM ARCHITECTURE** **3/0/3**
(Updated Fall 2020) **UK LEVEL: 4**
**UK CREDITS: 15**

| | |
|---|---|
| **PREREQUISITES:** | ITC 1070 Information Technology Fundamentals |
| **COREQUISITES:** | None. |
| **CATALOG DESCRIPTION:** | Computer architecture. Digital circuits and components. Types of data representation. Computer organisations and design. Logic design. |
| **RATIONALE:** | The course is designed to introduce students to the design of computer hardware. Emphasis is placed on microcomputer architecture techniques. The course is suitable for students who aim for a career in computer science, information technology, computer hardware engineering. |
| **LEARNING OUTCOMES:** | As a result of taking this course, the student should be able to:<br>1. Distinguish among numeric systems and data representation coding schemes.<br>2. Explain, identify and construct digital logic circuits.<br>3. Outline the design of combinational and sequential circuits.<br>4. Define the different memory types. |
| **METHOD OF TEACHING AND LEARNING:** | In congruence with the teaching and learning strategy of the college, the following tools are used:<br>• Classroom lectures, discussions, and review of real-world cases based on specific theoretical concepts. Laboratory practical sessions.<br>• Office hours: Students are encouraged to make full use of the office hours of their instructor, where they can ask questions and go over lecture material.<br>• Use of the Blackboard Learning platform, where instructors post lecture notes, assignment instructions, timely announcements, as well as additional resources. |
| **ASSESSMENT:** | **Summative:**<br>1st assessment: Coursework design and implementation of a digital circuit. **30%**<br>2nd assessment: Portfolio of student work and oral assessment **10%**<br>Final assessment: Final exam short essay questions and mathematical problems **60%**<br><br>**Formative:**<br>In-class and take home short problems, questions and mathematical problems **0%**<br><br>The formative assessments aim to prepare students for the summative assessments and expose them to teamwork.<br>The 1st summative assessment tests the LOs 1, 2, 3.<br>The 2nd summative assessment tests the LOs 1-4.<br>The final summative assessment tests the LOs 1-4.<br><br>*The final grade for this module will be determined by averaging all* |

| | |
|---|---|
| | *summative assessment grades, based on predetermined weights for each assessment. If students pass the **final summative assessment,** which tests all Learning Outcomes for this module, and the average grade for the module is 40 or above, students are not required to resit any failed assessments.* |
| **INDICATIVE READING:** | **REQUIRED READING:**<br>1. Mano, M. (1992). *Computer System Architecture* (3rd edition). Prentice-Hall<br><br>**RECOMMENDED READING:**<br>1. Booth Grayce M. (1980). *The Distributed System Environment*, McGraw Hill.<br>2. Marcovitz B. Alan (2009). *Introduction to Logic Design* (3rd edition), McGraw Hill.<br>3. Stallings William (2012). *Computer Organization and Architecture* (9th edition), Prentice Hall.<br>4. Stone Harold (1980). *Introduction to Computer Architecture,* Science Research Associates.<br>5. Willis N., Kerridge J. (1983). *Introduction to Computer Architecture,* Pitman. |
| **INDICATIVE MATERIAL:**<br>*(e.g. audiovisual, digital material, etc.)* | **REQUIRED MATERIAL:** N/A<br><br>**RECOMMENDED MATERIAL:**N/A |
| **COMMUNICATION REQUIREMENTS:** | Daily access to the course's site on the College's Blackboard CMS.<br>Communication using proper written and oral English.<br>Use of word processing and/or presentation graphics software for documentation of assignments. |
| **SOFTWARE REQUIREMENTS:** | MS-Office<br>Cedar Logic<br>MS-Visio |
| **WWW RESOURCES:** | Computer Organization and Design Course Web Site:<br>http://williamstallings.com/COA5e.html |
| **INDICATIVE CONTENT:** | 1. DIGITAL LOGIC CIRCUITS<br>1.1. Digital computers<br>1.2. Logic gates<br>1.3. Boolean algebra<br>1.4. Map simplification<br>1.5. Combinational circuits and flip flops<br>1.6. Sequential circuits<br>2. DIGITAL COMPONENTS<br>2.1. Integrated circuits<br>2.2. Decoders<br>2.2.1. NAND gate decoder and decoder expansion<br>2.2.2. Encoders<br>2.3. Multiplexers<br>2.4. Registers<br>2.5. Binary counters<br>2.6. Memory unit<br>3. DATA REPRESENTATION |

| | |
|---|---|
| | 3.1. Data types<br>3.1.1. Octal and hexadecimal numbers<br>3.1.2. Decimal and alphanumeric representation<br>3.2. Complements<br>4. REGISTER TRANSFER AND MICROOPERATIONS<br>4.1. Register transfer<br>4.2. Bus and memory transfers<br>4.3. Arithmetic microoperations<br>4.3.1. Binary adder, adder-subtractor, and incrementer<br>4.3.2. Arithmetic circuit<br>4.4. Logic microoperations<br>4.4.1. List of logic microoperations<br>4.4.2. Hardware implementation<br>4.5. Shift microoperations<br>4.6. Arithmetic logic shift unit<br>5. BASIC COMPUTER ORGANIZATION AND DESIGN<br>5.1. Instruction codes<br>5.2. Computer registers<br>5.3. Computer instructions<br>5.4. Timing and control<br>5.5. Instruction cycle<br>5.6. Memory-reference instructions<br>5.7. Input-output and interrupt<br>5.8. Design of basic computer<br>5.8.1. Control logic gates<br>5.8.2. Control of registers and memory<br>5.8.3. Control of flip-flops and common bus<br>5.9. Design of accumulator logic<br>6. MEMORY ORGANIZATION<br>6.1. Memory hierarchy<br>6.2. Main memory<br>6.2.1. Ram and rom chips<br>6.2.2. Memory address map<br>6.2.3. Memory connection to CPU<br>6.3. Auxiliary storage<br>6.4. Cache memory mapping and initialization<br>6.5. Virtual memory mapping and page replacement<br>6.6. Memory management hardware<br>6.6.1. Segmented-page mapping<br>6.6.2. Memory protection |