DEREE COLLEGE SYLLABUS FOR:

ITC 2086 COMPUTER SYSTEM ARCHITECTURE **3/0/3**
(Previously: ITC 2186 COMPUTER SYSTEM ARCHITECTURE) **UK LEVEL: 4**
(Updated Fall 2023) **UK CREDITS: 15**

PREREQUISITES:	None.
COREQUISITES:	None.
CATALOG DESCRIPTION:	Computer architecture. Digital circuits and components. Types of data representation. Computer organisations and design. Logic design.
RATIONALE:	The course is designed to introduce students to the design of computer hardware. Emphasis is placed on microcomputer architecture techniques. The course is suitable for students who aim for a career in computer science, information technology, computer hardware engineering.
LEARNING OUTCOMES:	As a result of taking this course, the student should be able to: 1. Distinguish among numeric systems and data representation coding schemes. 2. Explain, identify and construct digital logic circuits. 3. Outline the design of combinational and sequential circuits. 4. Define the different memory types.
METHOD OF TEACHING AND LEARNING:	In congruence with the teaching and learning strategy of the college, the following tools are used: • Classroom lectures, discussions, and review of real-world cases based on specific theoretical concepts. Laboratory practical sessions. • Office hours: Students are encouraged to make full use of the office hours of their instructor, where they can ask questions and go over lecture material. • Use of the Blackboard Learning platform, where instructors post lecture notes, assignment instructions, timely announcements, as well as additional resources.
ASSESSMENT:	**Summative:** 1st assessment: Coursework design and implementation of a digital circuit. **30%** 2nd assessment: Portfolio of student work and oral assessment **10%** Final assessment: Final exam short essay questions and mathematical problems **60%** **Formative:** In-class and take home short problems, questions and mathematical problems **0%** The formative assessments aim to prepare students for the summative assessments and expose them to teamwork. The 1st summative assessment tests the LOs 1, 2, 3. The 2nd summative assessment tests the LOs 1-4. The final summative assessment tests the LOs 1-4. *The final grade for this module will be determined by averaging all*

	*summative assessment grades, based on predetermined weights for each assessment. If students pass the **final summative assessment,** which tests all Learning Outcomes for this module, and the average grade for the module is 40 or above, students are not required to resit any failed assessments.*
INDICATIVE READING:	**REQUIRED READING:** 1. Mano, M, Kime, C, Martin T. (2016). *Logic and Computer Design Fundamentals* (5th edition). Pearson. **RECOMMENDED READING:** 1. Mano, M. (1992). *Computer System Architecture* (3rd edition). Prentice-Hall Booth Grayce M. (1980). *The Distributed System Environment*, McGraw Hill. 2. Marcovitz B. Alan (2009). *Introduction to Logic Design* (3rd edition), McGraw Hill. 3. Stallings William (2012). *Computer Organization and Architecture* (9th edition), Prentice Hall. 4. Stone Harold (1980). *Introduction to Computer Architecture,* Science Research Associates. 5. Willis N., Kerridge J. (1983). *Introduction to Computer Architecture,* Pitman.
INDICATIVE MATERIAL: *(e.g. audiovisual, digital material, etc.)*	**REQUIRED MATERIAL:** N/A **RECOMMENDED MATERIAL:**N/A
COMMUNICATION REQUIREMENTS:	Daily access to the course's site on the College's Blackboard CMS. Communication using proper written and oral English. Use of word processing and/or presentation graphics software for documentation of assignments.
SOFTWARE REQUIREMENTS:	MS-Office Cedar Logic MS-Visio
WWW RESOURCES:	Computer Organization and Design Course Web Site: http://williamstallings.com/COA5e.html
INDICATIVE CONTENT:	1. DIGITAL LOGIC CIRCUITS 1.1. Digital computers 1.2. Logic gates 1.3. Boolean algebra 1.4. Map simplification 1.5. Combinational circuits and flip flops 1.6. Sequential circuits 2. DIGITAL COMPONENTS 2.1. Integrated circuits 2.2. Decoders 2.2.1. NAND gate decoder and decoder expansion 2.2.2. Encoders 2.3. Multiplexers 2.4. Registers 2.5. Binary counters 2.6. Memory unit

	3. DATA REPRESENTATION 3.1. Data types 3.1.1. Octal and hexadecimal numbers 3.1.2. Decimal and alphanumeric representation 3.2. Complements 4. REGISTER TRANSFER AND MICROOPERATIONS 4.1. Register transfer 4.2. Bus and memory transfers 4.3. Arithmetic microoperations 4.3.1. Binary adder, adder-subtractor, and incrementer 4.3.2. Arithmetic circuit 4.4. Logic microoperations 4.4.1. List of logic microoperations 4.4.2. Hardware implementation 4.5. Shift microoperations 4.6. Arithmetic logic shift unit 5. BASIC COMPUTER ORGANIZATION AND DESIGN 5.1. Instruction codes 5.2. Computer registers 5.3. Computer instructions 5.4. Timing and control 5.5. Instruction cycle 5.6. Memory-reference instructions 5.7. Input-output and interrupt 5.8. Design of basic computer 5.8.1. Control logic gates 5.8.2. Control of registers and memory 5.8.3. Control of flip-flops and common bus 5.9. Design of accumulator logic 6. MEMORY ORGANIZATION 6.1. Memory hierarchy 6.2. Main memory 6.2.1. Ram and rom chips 6.2.2. Memory address map 6.2.3. Memory connection to CPU 6.3. Auxiliary storage 6.4. Cache memory mapping and initialization 6.5. Virtual memory mapping and page replacement 6.6. Memory management hardware 6.6.1. Segmented-page mapping 6.6.2. Memory protection